UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,045	12/31/2001	Hahn Vo	H052617.1142US0	2278

7590 01/26/2005

HEWLETT-PACKARD COMPANY
INTELLECTUAL PROPERTY ADMINISTRATION
P.O. BOX 272400
FORT COLLINS, CO 80527-2400

EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,045	VO, HAHN	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 22-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-36* is/are allowed.

6)☒ Claim(s) *1-5,9-17,20 and 37-42* is/are rejected.

7)☒ Claim(s) *6-8,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed 10/28/2004.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-9 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vartti et al. (US PAT. 5,678,026 hereinafter Vartti) in view of Hanawa et al. (US PAT. 5,740,401 hereinafter Hanawa).

Regarding claim 1, Vartti discloses a method of controlling access to a shared memory (10, figure 1) of a multiprocessor system (col. 5, lines 59-60), the multiprocessor system comprising a first bus and a second bus coupled to the shared memory, the first bus coupled to a first processor and the second bus coupled to a second processor (col. 6 lines 5-19), the method comprising the steps of requesting exclusive access to a first memory location of the shared memory by the first processor and granting exclusive access to the first memory location of the shared memory to the first processor (col. 6 line 20 through col. 8 line 16). Vartti differs from the claimed invention in not specifically teaches the steps of allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive

access to the first memory location and storing access request associated with the exclusive access in a first register in a first memory controller and in a second register in a second memory controller. However, Hanawa teaches a multiprocessor system including a control method in which acceptance of a memory access request, given from another processor, to data in a shared memory other than shared data being permitted while a first processor make access to the shared data in the shared memory and storing access request in a corresponding memory controller in order to access different address in parallel while exclusive access is currently made, thereby improving the throughput of the bus (col. 2 line 15 through col. 4 line 10 and col. 6 line 41 through col. 8 line 62). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Hanawa in having the steps of allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive access to the first memory location and storing access request associated with the exclusive access in a first register in a first memory controller and in a second register in a second memory controller, as per teaching of Hanawa, in order to access different address in parallel while exclusive access is currently made.

Regarding claim 2, Hanawa discloses to request exclusive access by asserting a lock signal on the first bus and sending a lock request from the first processor (110, figure 1) to the first memory controller (500, figure 1) coupled to the first bus, the second bus, and the shared memory (col. 11 line 62 through col. 12 line 7).

Regarding claim 4, Hanawa teaches to forward the lock request from the first memory controller to a switch (506, figure 7), and signaling the first processor to retry the lock request (col. 13 line 61 through col. 14 line 6).

Regarding claim 5, Hanawa teaches to grant exclusive access by signaling the first memory controller by the switch to retry the lock request (col. 13 line 61 through col. 14 line 6), assigning exclusive access to the first memory location by the switch by determining if the first memory location is currently assigned, saving a lock request information if the first memory location is not currently assigned and sending the lock request information to the memory controller (col. 14 lines 14-51), notifying the first memory controller of the exclusive access assigned in the assigning step and granting exclusive access to the first memory location by the memory controller responsive to a retry of the lock request by the first processor (col. 14 liens 51-67).

Regarding claim 9, Vartti teaches to release exclusive access to the first memory location (col. 8 lines 9-16).

Regarding claim 37, Vartti teaches to route the access request information to a remote out priority circuit from a first memory controller to a second memory controller (col. 7 line 56 through col. 8 line 16) so that one skill in the art would recognize Vartti teaches the request information in the second memory controller being a shadow copy of access request information in the first controller.

4. Claims 10-12, 14-17 and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vartti et al. (US PAT. 5,678,026 hereinafter Vartti) in view of Hanawa et al. (US PAT. 5,740,401 hereinafter Hanawa) and Lindeman (US PAT. 6,105,094).

Regarding claim 10, Vartti discloses a method of controlling access to a shared memory (10, figure 1) of a multinodal system (col. 5, lines 59-60), the multinodal system comprising a

plurality of multiprocessor node (col. 6 lines 5-19), the method comprising the steps of requesting exclusive access to a first memory location of the shared memory in a first multiprocessor node of the plurality of multiprocessor node by a first processor of the first multiprocessor node and granting exclusive access to the first memory location of the shared memory to the first processor (col. 6 line 20 through col. 8 line 16). In addition, Vartti teaches to route the access request information to a remote out priority circuit from a first memory controller to a second memory controller (col. 7 line 56 through col. 8 line 16) so that the multinodal system capable of sending access request information associated with the exclusive access of the shared memory of the first multiprocessor node to the second multiprocessor node. Vartti differs from the claimed invention in not specifically teaches the steps of allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive access to the first memory location. However, Hanawa teaches a multiprocessor system including a control method in which acceptance of a memory access request, given from another processor, to data in a shared memory other than shared data being permitted while a first processor make access to the shared data in the shared memory in order to access different address in parallel while exclusive access is currently made, thereby improving the throughput of the bus (col. 2 line 15 through col. 4 line 10 and col. 6 line 41 through col. 8 line 62). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Hanawa in having the steps of allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive access to the first memory location, as per teaching of Hanawa, in order to access different address in parallel while exclusive access is currently made. Furthermore, neither Vartti

nor Hanawa specifically teaches communicating between the multiprocessor node through a switch and sending access request information associated with the exclusive access of shared memory of the first multiprocessor node to the second multiprocessor node by the switch. However, Lindeman teaches a method for allocating exclusive shared resource in a computer system comprising an access arbiter unit functioning as a switch communicating between multiprocessor node in order to guarantee the bandwidth of data transfer (col. 7 lines 9-61). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Vartti and Hanawa in having communicating between the multiprocessor node through a switch and sending access request information associated with the exclusive access of shared memory of the first multiprocessor node to the second multiprocessor node by the switch, as per teaching of Lindeman, in order to guarantee the bandwidth of data transfer.

Regarding claim 11, the limitation of the claim is rejected as the same reasons set forth in claims 2 and 4.

Regarding claim 12, Vartti discloses the shared memory comprising memory subsystem 1 coupled to first storage controller and memory subsystem 2 coupled to a second storage controller of a different multiprocessor node of the plurality of multiprocessor nodes (figure 1).

Regarding claims 14-15, Hanawa discloses the first memory address data referencing the first memory (130, figure 1) or the second memory and the second memory address referencing the second memory (140, figure 1) or the first memory (col. 5 lines 39-45 and col. 7 lines 53-63).

Regarding claim 16, the limitation of the claim is rejected as the same reasons set forth in claim 4.

Regarding claim 17, the limitation of the claim is rejected as the same reasons set forth in claim 5.

Regarding claim 38, Vartti teaches to forwarding the access request information to the second memory controller in the second multiprocessor node and storing the access request information in the second memory controller (col. 7 line 56 through col. 8 line 16). Although Vartti does not specifically teach to forward the access request information via the switch, Lindeman teaches a method for allocating exclusive shared resource in a computer system comprising an access arbiter unit functioning as a switch communicating between multiprocessor node in order to guarantee the bandwidth of data transfer (col. 7 lines 9-61). Thus, the combination of Vartti, Hanawa and Lindeman is enough to reject the claimed limitations.

Regarding claim 39, Hanawa teaches to store the access information in a first register of a first memory controller in the first multiprocessor node and in a second register in the second memory controller (col. 7 lines 53-63).

Regarding claim 40, Vartti teaches to route the access request information to a remote out priority circuit from a first memory controller to a second memory controller (col. 7 line 56 through col. 8 line 16) so that one skill in the art would recognize Vartti teaches the request information in the second memory controller being a shadow copy of access request information in the first controller.

Regarding claim 41, the limitations of the claim are rejected as the same reasons as set forth in claim 10.

Regarding claim 42, the limitations of the claim are rejected as the same reasons as set forth in claim 40.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vartti et al. (US PAT. 5,678,026 hereinafter Vartti) in view of Hanawa et al. (US PAT. 5,740,401 hereinafter Hanawa) in view of Schibinger et al. (US PAT. 6,092,156 hereinafter Schibinger).

Regarding claim 3, the combination of Vartti and Hawana differs from the claimed invention in not specifically teaching to assert a lock signal by asserting a split lock signal on the first bus, wherein the split lock signal indicating that the lock request contains two memory address data. However, Schibinger teaches a method for avoiding deadlocks utilizing split lock operation to provide exclusive access to memory by asserting a split lock signal on a bus (520, figure 5), wherein the split lock signal indicating that the lock request contains more than one cache line (col. 8 lines 17-34). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Vartti and Hawana in asserting the split lock signal on the first bus, wherein the split lock signal indicating that the lock request contains two memory address data, as per teaching of Schibinger, in order to provide exclusive access to memory for avoiding deadlocks.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vartti et al. (US PAT. 5,678,026 hereinafter Vartti) and Hanawa et al. (US PAT. 5,740,401 hereinafter Hanawa) in view of Lindeman (US PAT. 6,105,094) and further in view of Schibinger et al. (US PAT. 6,092,156 hereinafter Schibinger).

Regarding claim 13, the combination of Vartti, Hanawa and Lindeman differs from the claimed invention in not specifically teaches to asserting a split lock signal on the first bus,

wherein the split lock signal indicating that the lock request contains two memory address data. However, Schibinger teaches a method for avoiding deadlocks utilizing split lock operation to provide exclusive access to memory by asserting a split lock signal on a bus (520, figure 5), wherein the split lock signal indicating that the lock request contains more than one cache line (col. 8 lines 17-34). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Vartti, Hanawa and Lindeman in asserting the split lock signal on the first bus, wherein the split lock signal indicating that the lock request contains two memory address data, as per teaching of Schibinger, in order to provide exclusive access to memory for avoiding deadlocks.

Allowable Subject Matter

7. Claims 6-8 and 18-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 22-36 are allowed.

Response to Arguments

9. Applicant's arguments filed 10/25/2004 have been fully considered but they are not persuasive.

In response to Applicant's argument of Hanawa failing to indicate or suggest that access request information associated with an exclusive access being stored in two different memory

controller, it is noted that Hanawa clearly teaches the access request is directed to the access queue of a corresponding memory controller (col. 7 lines 53-63) so that one skill in the art would recognizes Hanawa teaching the step of storing access request associated with the exclusive access in a first register in a first memory controller and in a second register in a second memory controller. Thus, the combination of Vartti and Hanawa is enough to reject claimed limitations.

10. Applicant's arguments with respect to claims 10-20 and 38-42 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 571-272-4183. The examiner can normally be reached on M-F 9:00am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
Art Unit 2186

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100